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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,864	03/15/2001	Jigish D. Trivedi	MIO 0079 PA	5568

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EXAMINER

FOONG, SUK SAN

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 02/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/808,864

Applicant(s)

TRIVEDI ET AL.

Examiner

Suk-San Foong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) 17-20, 29 and 30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-16 and 21-28 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Election/Restrictions

1. The restriction between 1st specie, 2nd specie, 3rd specie and 4th specie is withdrawn because the species are not now seen to be patentably distinct.

Specification

2. The disclosure is objected to because of the following informalities: it appears that “polycilicide” should be replaced by--polysilicide--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-16 and 21-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 1, and other occurrences, it appears that “polycilicide” should be replaced by--polysilicide--.

6. Claim 1, and other occurrences, it is not clear what is recited through the term “substantial”.

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7. Claims 21-26, it is not clear what is recited through the term “ultrathin”.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 1-3, 6-11, 13-16 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in combination with Kizilyalli et al. ('807).

AAPA admits to a SRAM device with CMOS structure 4 substantially as claimed to have been known prior to applicant's invention with the exclusion of a diffusion barrier layer formed

between a portion of polysilicon layer and metal, metal silicide or metal nitride film (Instant Figs. 1 and 2, and page 8, line 12 to page 9, line 15).

Kizilyalli et al. discloses a semiconductor structure for a memory device such as SRAM which includes semiconductor substrate 16 (Col. 2, line 49, and Fig. 1), P-well 24 and N-well 26 in substrate 16 (Col. 2, lines 49-50), isolation region 28 that isolates active regions formed in respective P-well 24 and N-well 26 (Col. 2, lines 53-57), and polysilicide gate electrode structure composed of polycrystalline silicon film 20 by formation of N+ polysilicon layer 30 located above P_r-well 24 followed by formation of P+ polysilicon layer 32 located above n-well region 36 (Col. 2, lines 57-60), diffusion barrier layer 50 formed over a portion of polysilicon film 20 wherein the portion includes N+ polysilicon layer 30 (Col. 2, line 60 to Col. 3, line 41, and Col. 4, lines 11-14) thereby blocking migration of P+ dopants through metal silicide film 60 over path 72 (Col. 4, lines 23-26 and lines 30-33) and blocking migration of N+ dopants through metal silicide film 60 and P+ polysilicon layer 32 over path 88 (Col. 4, lines 34-37, and Fig. 5) and metal silicide film 60 formed over polysilicon film 20 (Col. 3, lines 66-67).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the AAPA with Kizilyalli et al. because it would enable formation of diffusion barrier layer 50 of Kizilyalli et al. in AAPA's CMOS structure 4 and obtain further advantage of minimizing dopant penetration and migration (Kizilyalli et al., Col. 1, lines 53-55).

The choice of thickness of the polycrystalline silicon film would have been a matter of routine optimization to achieve the desired device density and the desired device characteristics of the device to be formed. (See MPEP 2144.05).

The choice of thickness of the diffusion barrier layer would have been a matter of routine optimization to achieve the desired device and the desired device characteristics of the device to be formed. (See MPEP 2144.05).

11. Claims 4, 5, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Kizilyalli et al. ('807) as applied to claims 1-3, 6-11, 13-16 and 21-26 above, and further in view of Fujii et al. ('010).

The combination does not disclose that the barrier layer does not extend over a portion of N+ polysilicon layer.

Fujii et al. discloses a CMOS structure which includes P-type semiconductor substrate 1 (Col. 3, lines 52-53), N-well 2 formed in substrate 1 (Col. 4, lines 4-7), isolation region 3 (Col. 4, lines 7-8), active areas 4 and 5 formed in P-type region of substrate 1 and N-well 2 (Col. 4, lines 9-13, and Fig. 2A), and polysilicide gate electrode structure composed of polysilicon layer 9 formed over gate oxide film 8 (Col. 4, lines 15-17), then first P+ doped region 9a is formed in a portion polysilicon layer 9 (Col. 4, lines 17-22), subsequently second N+ doped region 9b is formed in a second portion of polysilicon layer 9 (Col. 4, lines 23-28, and Fig. 2B), and metal silicide layer 12 over polysilicon layer 9 (Col. 4, lines 29-31, and Fig. 2C).

In view of the disclosure of Kizilyalli et al. wherein diffusion barrier layer 50 is formed over first doped region 30 in polysilicon film 20 in order to prevent subsequent introduction of a second dopant to form second doped region 32 (Col. 3, lines 55-65, and Fig. 3), it would have been within the scope to one ordinary skill in the art to combine the teachings of Fujii et al. with the combination because it would enable formation of a diffusion barrier layer over P+

polysilicon layer 22 of AAPA in the combination to be performed and obtain further advantage of minimizing dopant penetration and migration (Kizilyalli et al., Col. 1, lines 53-55).

12. Claims 1-3, 6, 9, 10-16 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in combination with Hunter et al. ('725).

AAPA admits to a SRAM device with CMOS structure 4 substantially as claimed to have been known prior to applicant's invention with the exclusion of a diffusion barrier layer formed between both doped regions of the polysilicon layer and metal, metal silicide or metal nitride film (Instant Figs. 1 and 2, and page 8, line 12 to page 9, line 15).

Hunter et al. discloses a semiconductor structure in semiconductor devices for inhibiting outdiffusion of dopants from a first conductive layer such as polycrystalline silicon to a second conductive layer such as silicide conductive material which includes a semiconductor substrate 36 and isolation region 34 (Col. 3, lines 57-58, and Fig. 2A), N-well 38 and P-well 40 formed in substrate 36 (Col. 3, lines 61-62), polysilicide gate electrode structure composed of polysilicon film 44 comprised of N+ polysilicon layer 45 and P+ polysilicon layer 46 (Col. 4, lines 4-8), diffusion barrier layer 48 formed on surface of polysilicon layer 44 (i.e. N+ polysilicon layer 45 and P+ polysilicon layer 46) (Col. 4, lines 12-15, and Fig. 2C) and conductive layer 50 such as metal silicide (Col. 4, lines 57-59, and Fig. 2D).

It would have been within the scope to one ordinary skill in the art to combine the teachings of AAPA with Hunter et al. because it would enable formation of diffusion barrier layer 48 in AAPA's CMOS structure 4 and obtain further advantage of inhibiting outdiffusion of

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dopants from polycrystalline silicon into silicide conductive layers (Hunter et al., Col. 2, lines 64-67).

The choice of thickness of the polycrystalline silicon film would have been a matter of routine optimization to achieve the desired device density and the desired device characteristics of the device to be formed. (See MPEP 2144.05).

The choice of thickness of the diffusion barrier layer would have been a matter of routine optimization to achieve the desired device and the desired device characteristics of the device to be formed. (See MPEP 2144.05).

Conclusion


13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.


February 7, 2003


George Hourson
Primary Examiner
Art Unit 2823